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# A chaotic circuit based on a physical memristor

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ABSTRACT

The memristor is a fundamental two-terminal electrical component unique in that it possesses the properties of non-linearity and memory, which are pervasive across natural systems. It has been proven to be in principle a viable substrate for novel dynamical systems showing chaotic behavior, but the recourse to abstract, idealized mathematical non-linearities throughout the existing literature hinders practical realization using physical devices. In this work, we realize a fully autonomous chaotic oscillator circuit based on self-directed channel memristors. Its architecture comprises two feedback loops, a linear one and a non-linear one involving the memristor. Low-dimensional chaotic dynamics are readily obtained experimentally using tungsten-based as well as carbon-based physical devices, despite their non-idealities. A mathematical model of the circuit, revealing further interesting non-linear features such as bifurcations without parameters, is also offered.



## 1. Introduction

In 1971 L.O. Chua, noticing the incompleteness of the relationships between the fundamental electrical quantities expressed by the resistor, capacitor, and inductor, postulated the existence of a fourth electrical component: he named it a memristor and defined it as a non-linear two-terminal element which relates electric charge with magnetic flux linkage [1]. A few years later, memristive systems, a class of non-linear dynamical systems generalizing memristors and having peculiar characteristics through being memory elements with frequency-dependent non-linear behavior and pinched hysteresis *i-v* loops, were introduced [2]. These two seminal studies led to the question of whether such systems were purely theoretical or useful as physical models of real components not yet identified or discovered. An answer was provided in 2008 by the work of D.B. Strukov and coauthors who, characterizing a new $TiO_2$ nanoscale device, discovered a current-voltage behavior that could be ascribed to memristive nature [3]. In turn, this work paved the way for a renewed interest in memristors and their applications across widely different fields.

Over the recent years, memristors, owing to the ability of hysteretically changing their resistance in response to previously-applied electrical stimuli [4,5], have attracted considerable interest for diverse hypothetical applications such as nonvolatile memories [6,7], logic gates [8–11], hybrid logic/memory circuits [5], and neuromorphic computing [12,13]. In particular, the unique prerogatives of the device fuel interest in evaluating it as a possibly optimal substrate for generating non-linear and chaotic dynamics [14–16]. Non-linear circuits based on memristors could potentially involve a reduced number of components, thus producing architectures that would be particularly simple, well-suited for large-scale replication and design of biologically-inspired systems [17–19]. However, despite all research efforts invested in this direction, there remains a wide gap between theoretical studies presenting memristor-based mathematical systems producing chaos or other non-linear behaviors, and their practical realizations confirming the actual suitability of physical memristive devices for any such purposes.

Countless chaotic oscillators based on memristors have been theorized starting from known topologies of chaotic or periodic circuits and substituting a non-linear or a linear component with a memristor or a memristive system. Several works are based on Chua's circuit or its variants, wherein the Chua's diode is replaced

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with a memristor [14,15,17,20,21]. Chaotic circuits have also been theorized from Shinriki's circuit [22] or from the jerk chaotic system [23] by using a first-order memristive diode bridge in place of the non-linear element, or in place of a resistor in active filters [24,25]. Finally, other memristive chaotic systems have been designed *ab initio* predicated on non-linear dynamics arguments and numerical simulations [18,26,27]. Importantly, the near-totality of these oscillators assume ideal characteristics for the memristor, such as cubic or piece-wise-linear non-linearities [14]. Consequently, any hypothetical laboratory implementation of these abstract mathematical systems must rely on analog emulators of the memristor, which often require a significant number of components, thus negating the appeal of a memristor-based approach in the first place [15,28].

A first step towards filling the gap between theoretical models and practical realizations is represented by chaotic oscillators using physics-based models of the memristors, such as Strukov's model [29,30]. These works rely on an architecture based on Chua's circuit and, to recover the symmetry of the non-linearity suitable for chaos generation starting from a component that is passive and non-symmetrical, utilize a configuration of two memristors connected in anti-parallel. A second step was the realization and experimental characterization of sub-circuits including one or more memristors alongside an external or internal driver [31–33]. In particular, in Ref. [31] memristors connected in series, parallel and anti-parallel configurations were considered, whereas in Ref. [32] feedback configurations using programmable source meters were presented; both works make use of flexible $TiO_2$ memristors constructed with spin-coating techniques and demonstrate non-linear dynamics such as spiking and chaotic time-series. In Ref. [33], a nanoscale $NbO_2$ Mott memristor was used, and chaotic dynamics were found as the result of the coupling with an intrinsic oscillator due to thermal fluctuations in the nanoscale volume, a mechanism inherently not observable in larger-scale devices. While providing evidence of the effective viability of physical memristors in generating non-linear dynamics, these works crucially did not offer a fully autonomous circuit architecture for chaotic oscillation, which is, instead, the main focus of the present contribution.

The design of a real, fully autonomous chaotic circuit based on a physical memristor is far from being a trivial task because experimental devices can significantly differ from the abstract non-linear functions which populate mathematical models of the oscillators. Besides, non-idealities, tolerances, technological constraints (for example, in having stringent limits to the voltage and current that they can tolerate) and instability, alongside limited reliability and lifetime of the currently available memristors, strongly impact the usability of many otherwise viable circuit topologies. It should also be taken into account that, while in digital applications specific SET and RESET procedures can be defined to overcome the non-idealities of the device, the effective use of a memristor in analog applications such as chaos generation is often enabled only by continuous exploitation of its non-linear features over the full range of operation.

For these reasons, in this paper, we have pursued a bottom-up approach, starting from a commercially available device and tailoring a realistic circuit architecture around its physical properties and limits. We report a circuit wherein the memristor is the only source of non-linearity, and the resulting architecture is based on three cascaded active linear RC filters with two feedback loops, one linear and one involving the memristor non-linearity. This circuit has been realized in the laboratory and characterized experimentally, proving its practical suitability for generating chaos. The numerical simulations of an idealized model complement the experimental results, qualitatively confirming the chaotic behavior observed and additionally highlighting the presence of non-linear phenomena common across the postulated memristor-based oscillators, such as multi-stability and bifurcation without parameters.

## 2. Physical memristor

Despite intense investment towards the identification of viable materials and reliable fabrication processes, to date, memristors have failed to become a mainstream electronic component, and their availability remains limited. For the present study, we have used the discrete commercial parts marketed by Knowm Inc. (Santa Fe NM, USA), which are commercially off-the-shelf available for mail order [34]. These are ion-conducting devices, referred to as self-directed channel (SDC) memristors, wherein the resistance change is determined by the movement of Ag+ ions inwards or outwards of agglomeration sites (e.g., channels) within the active layer. The conductive channels are generated via dopant-catalyzed reactions, and, depending on the dopant used, either tungsten or carbon, two device types are available with different electrical characteristics [35,36].

Independent discrete memristors are packaged as groups of 8 into 16-pin ceramic DIP-packages. Upon receipt, they are not generally formed, so a forming process was carried out, which consisted of applying a $f = 2$ Hz sine-wave, whose amplitude was gradually increased from $v = 0$ to 1 $V_{pp}$ over 5 min. This process releases Sn ions from the SnSe layer and forces them into the active layer, wherein they support the incorporation of $Ag^{+}$ ions. Similar results are obtained with other frequencies on the same order, but gradually increasing the applied voltage up to a level comparable to that found in the oscillator circuit is essential. To limit the current, a series resistor $R_1 = 10$ kΩ or 47 kΩ was inserted, respectively, for the tungsten- and carbon-based devices. During the forming process, a minority of devices fail to develop the pinched *i-v* hysteresis loop, often behaving instead as a high-valued resistor. This situation could also arise after successful forming, either as a gradual drift or a sudden event, in which case a rescue procedure consisting of repeatedly applying a $\pm$ 3 V potential for few seconds was attempted [36]. As the devices are extremely fragile, all procedures were completed at a static-safe workstation.

The complexity of the physical device readily became apparent through applying a sine-wave of varying amplitude and frequency after forming. For brevity, only the example case of one tungsten-based device is presented. As visible in Fig. 1a, during elevating the voltage of a $f = 2$ Hz wave from $v = 0.6$ to 2.4 $V_{pp}$, the qualitative features of the loop changed appreciably. While the slope corresponding to $1/R_{off}$ remained approximately unchanged and that corresponding $1/R_{on}$ became steeper, the loop area increased more markedly within the negative than the positive quadrant, its trajectory therein becoming progressively less smooth and more reminiscent of a triangle. Keeping all settings unchanged and increasing the frequency to 4 Hz and 8 Hz (Fig. 1b and c, respectively), even greater complexity could be revealed, whereby the morphology of the loop was further distorted and rendered more clearly sensitive to the applied voltage, affecting both the shape and the area within both quadrants in non-trivial ways.

Furthermore, comparing, as shown in Fig. 1d, the loops acquired at $v = 2$ $V_{pp}$ and $f = 8$ Hz before and after 30 min comprising both external driving and oscillatory operation, revealed an apparent non-volatile effect. The slope corresponding to $1/R_{off}$ increased, the loop shrank and the shape of both lobes was clearly altered. Eventually, the loop shrinks into a line such that the device loses its non-linear and memory properties, collapsing into a resistor having $R_{on} \approx R_{off}$. While this could oftentimes be relieved via transient application of a biasing voltage, the properties of pristine devices could not be fully recovered. Finally, taking as an example the case of $v = 1.2$ $V_{pp}$ and $f = 8$ Hz, considerable cycle-to-cycle current variations could be seen, delineating an unstable or-

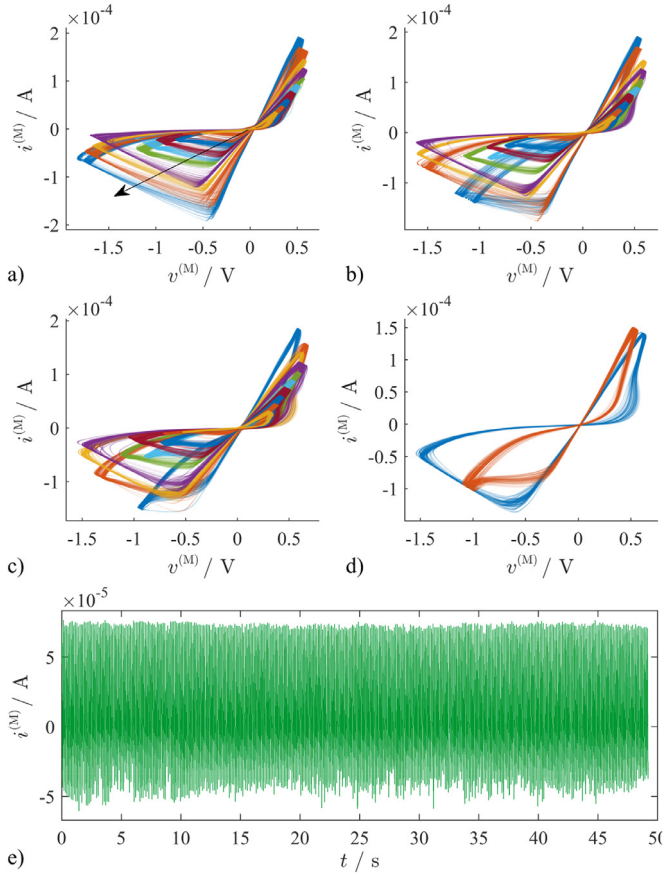


**Fig. 1.** Loops and waveform experimentally acquired during sinusoidal driving of a representative tungsten-based memristor specimen. a), b) and c) Effect of increasing the applied voltage $v = \{0.6, 0.8 \ldots 2.4\} V_{pp}$, as denoted by the arrow, separately for $f = \{2, 4, 8\}$ Hz respectively. d) Non-volatile change in the device parameters, shown for $v = 2$ $V_{pp}$ and $f = 8$ Hz, wherein blue and orange denote measurements taken, respectively, before and after a 30-minute operation interval. e) Unstable time-course of current while driving at $v = 1.2$ $V_{pp}$ and $f = 8$ Hz. $i^{(M)}$ and $v^{(M)}$ denote, respectively, the current through and the voltage across the device under test. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

bit (Fig. 1e); though this effect was observed inconsistently, it exemplifies the complexity of the dynamical properties available to the physical devices, which can emerge even when an isolated one is simply periodically forced.

Together with manufacturing variability, not reported for brevity, these non-idealities delineate profound differences between a physical memristor and one simulated numerically or electronically via an op-amp based non-linear topology. Unlike a digital circuit such as a logic gate, a chaotic oscillator explores the continuous range of values, and is inherently sensitive to parameter settings, implying that these aspects considerably impact the design of a viable circuit.

## 3. Experimental oscillator circuit

Ahead of introducing the designed circuit, some considerations are outlined, which stem from extensive preliminary experimentation with these devices and here served to narrow down the range of possible candidate topologies considerably. Firstly, according to the manufacturer, there are stringent requirements of maximum voltage across and current through the memristor: the former is $\pm$ 3 V, whereas the latter is $\pm$ 1 mA for tungsten-based and $\pm$ 0.05 mA for carbon-based parts. Even during short transients, exceeding these values causes complex and potentially irreversible alterations to the active layer, including phase-change effects [36]. Consequently, a practically-viable circuit requires that the self-directed channel memristor is connected in series to a suitably large current-limiting resistor, prohibiting secondary paths through reactive devices. For this reason, straightforwardly replacing the nonlinear element with a memristor into architectures, e.g., derived by the Chua's circuit and its variants [14,15,17,20,21], may yield an experimental realization that causes device damage or otherwise fails at generating chaotic behavior.

Secondly, a circuit that does not tend to saturate quickly is required, since the application of an asymmetric potential causes a lasting drift in the memristor parameters and, depending on the power supply voltage, saturation can easily lead to the maximum voltage limit being exceeded. On the other hand, introducing other non-linear elements such as Zener diodes or varistors as protection means would complicate ascribing the emergent dynamics to the memristor itself. Thirdly, because many factors, including non-volatile effects, influence the non-linear curve, a circuit which can generate chaos over a sufficiently large region of the parameter space is required. Otherwise, there is the risk that, even if chaotic operation is attained, it only manifests as a transient because phase transition causes different driving of the memristor, which in turn responds by altering its properties, thus shifting to another non-chaotic region of the parameter space. The second and third considerations together underline criticalities that can arise in those circuits designed for memristors electronically-simulated and, hence, free from non-volatile effects [24,25], ultimately orienting the choice of the candidate circuit topology towards robust chaotic architectures.

Based on these considerations, the jerk circuit introduced in 2011 by J.C. Sprott was identified as a suitable starting point, particularly given that, by construction, it is chaotic over a broad range of component values, and poses minimal requirements on the shape of the non-linearity. It was initially intended for use with a diode, and consists of three cascaded op-amp-based integrator stages, effectively realizing a linear and a non-linear feedback loop [37]. Here, as shown in Fig. 2a, it was adopted for operation with a memristor, with some adjustments. Namely, the top-left op-amp circuit containing the memristor $M$ replaces the diode; therein, the current-limiting resistor was empirically set to $R_1 = 68$ kΩ and $R_1 = 100$ kΩ for the tungsten- and carbon-based devices respectively. While conceptually superfluous, $R_2$ avoids possible damage due to transient over-current flowing through the protection diodes of the inverting input during power-up. The offset voltage $U$ serves as a secondary control parameter and was manually adjusted, steering the memristor non-linearity towards persistent chaotic operation, eventually reaching $U = 0.43$ V and $U = 0.55$ V for the tungsten- and carbon-based devices, respectively, in the cases shown. At the output of this op-amp, the memristor non-linearity manifests itself in positive voltage spikes. The remainder of the initial circuit was left unchanged, except that additional gain-setting resistors were added in parallel to the capacitors, effectively turning all integrator stages into active $RC$ filters.

In the final circuit, visible in Fig. 2a, the linear feedback loop comprises all three cascaded stages, whose output $v_2$ is fed back to the first stage via the resistor $R_9$. In the non-linear feedback loop, the output $v_3$ of the second stage enters a separate gain stage whose output, in turn, sets the voltage across the memristor through an operational amplifier in voltage-follower configuration. The memristor current flows entirely through the resistor $R_1$, thus contributing with a non-linear term to the voltage signal $v_4$, which sums the offset $U$, the memristor voltage $v^{(M)}$ and the voltage drop $R_1 i^{(M)}$. This signal closes the non-linear feedback loop by entering the first $RC$ stage through the variable resistor $R_3$, which acts as the primary control parameter throughout the experiments. While in the initial circuit $C_1 = C_2 = C_3$, here $C_1 = C_3 \approx 2C_2$, further

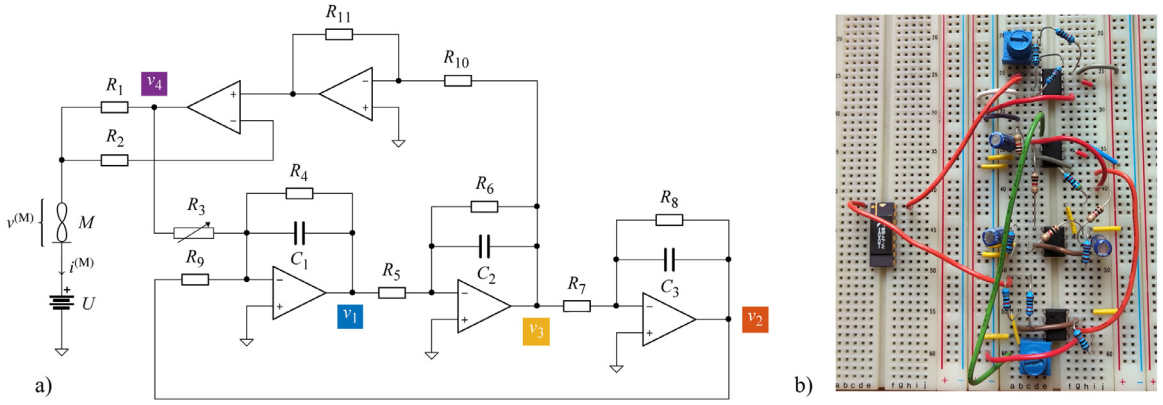


**Fig. 2.** The proposed chaotic oscillator based on a self-directed channel memristor. a) Schematic of the circuit. b) Picture of the physical realization, showing the ceramic-packaged memristor on the left. The top and bottom potentiometers on the right control, respectively, $U$ and $R_3$. The nominal component values ( ± 5% and ± 10% tolerance for $R$ and $C$, respectively) were set to $R_2$ = 10 kΩ, $R_3$ = 3.7 kΩ, $R_4$ = $R_5$ = $R_7$ = $R_9$= 1 kΩ, $R_6$ = 22 kΩ, $R_8$ = 33 kΩ, $R_{10}$=47 kΩ, $R_{11}$=100 kΩ, $C_1$ = $C_3$ = 47 μF, and $C_2$ = 22 μF. $R_1$ was set to $R_1$=68 kΩ and $R_1$=100 kΩ for experiments with the tungsten- and carbon-based devices; accordingly, the offset was set to $U$ = 0.43 V and $U$ = 0.55 V. All operational amplifiers are type TL082 (STmicroelectronics SpA, Agrate Brianza MI, Italy). Power supply is ± 8 V. Signal recording probes were removed for clarity.

shaping the frequency response of both loops. This choice, as well as the determination of the other component values, may be not critical and was driven by comprehensive preliminary experiments conducted using the tungsten-based memristor.

Applying Kirchhoff's laws and the relationships valid for ideal operational amplifiers, one gets

$$\begin{cases} \frac{dv_1}{dt} &= \frac{1}{C_1}\left(-\frac{v_1}{R_4}-\frac{v_2}{R_9}-\frac{v_4}{R_3}\right) \\ \frac{dv_2}{dt} &= \frac{1}{C_3}\left(-\frac{v_2}{R_8}-\frac{v_3}{R_7}\right), \\ \frac{dv_3}{dt} &= \frac{1}{C_2}\left(-\frac{v_1}{R_5}-\frac{v_3}{R_6}\right) \end{cases} \tag{1}$$

where

$$v_4 = -\frac{R_{11}}{R_{10}}v_3 + R_1 i^{(M)}; \tag{2}$$

it should be borne in mind that, as clarified in Sec. IV, the relationship between $v^{(M)}$ and $i^{(M)}$ involves a fourth state variable internal to the memristor.

Owing to its structural simplicity and the absence of any high-frequency or high-impedance nodes, the circuit was constructed on a plug-board using type TL082 operational amplifiers, discrete resistors, and capacitors, alongside two potentiometers controlling $U$ and $R_3$, and the memristors described in Section 2. Signals at the relevant nodes, including $v_1$, $v_2$, $v_3$, $v_4$ and the memristor terminals, were digitized at 16-bit, 5 kSa/s using a data acquisition card (type U2353A, Keysight Inc., Santa Rosa CA, USA) for 480 s, yielding 2.4 million points per run. The viability of the circuit for chaos generation was tested repeatedly using three tungsten-based and three carbon-based memristors, confirming the reproducibility of the findings. Here, for brevity, only one representative example of each is presented, and the corresponding raw data are freely available from Ref. [38]. It should be noted that $U$ and $R_3$ had to be tuned manually using a heuristic procedure, to account not only for the manufacturing and forming variability but also for minor variations in the trajectory of the manual adjustment process, which eventually impacted the memristor parameters.

Visual inspection of the time-series for $v_1$, $v_2$, $v_3$ and $v_4$ (Figs. 3a and 4a) revealed irregular oscillation, manifest primarily with cycle amplitude fluctuations alongside a strong harmonic component, which was readily apparent also in the frequency

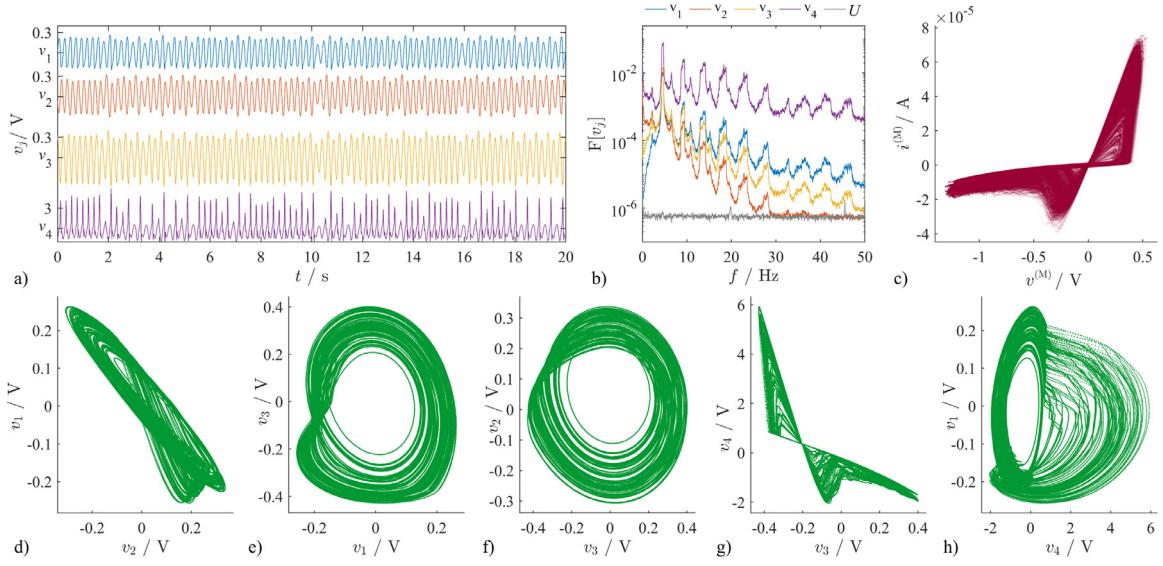


**Fig. 3.** Experimental results from the tungsten-based memristor. a) Time-series of the node voltages $v_1 \ldots v_4$. b) Corresponding frequency spectra, wherein the source $U$, set to a constant voltage, is additionally shown to represent the recorded noise baseline. c) Current-voltage plot of the pinched hysteresis loop. d-h) Projections of the attractor onto multiple planes.

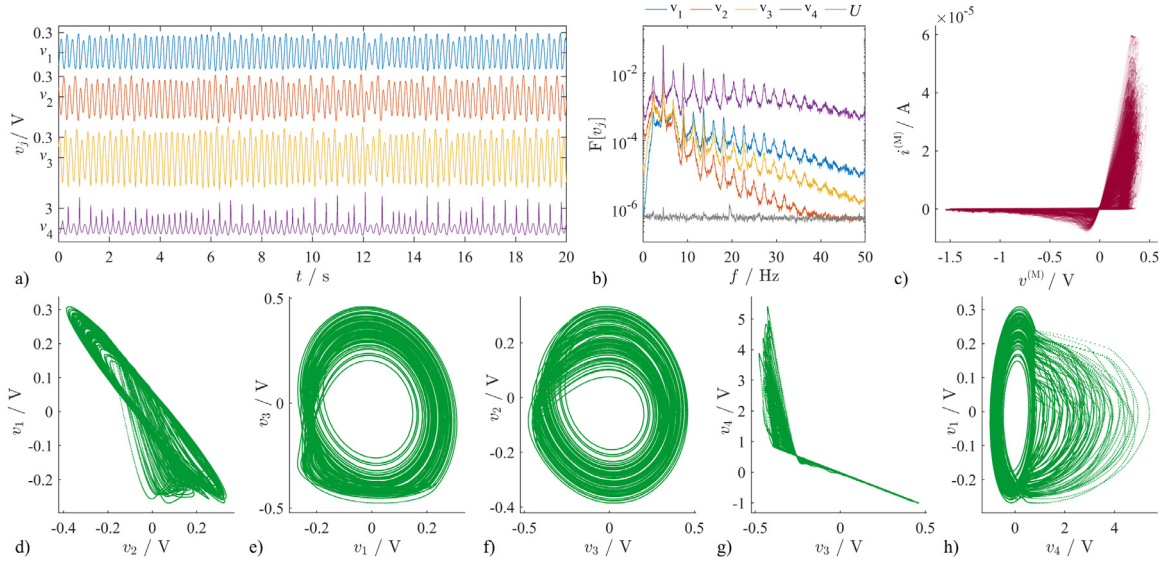


**Fig. 4.** Experimental results from the carbon-based memristor. a) Time-series of the node voltages $v_1 \dots v_4$. b) Corresponding frequency spectra, wherein the source $U$, set to a constant voltage, is additionally shown to represent the recorded noise baseline. c) Current-voltage plot of the pinched hysteresis loop. d-h) Projections of the attractor onto multiple planes.

spectra (Figs. 3b and 4b). For both realizations, the broadband spectra featured a dominant peak at $\approx 5$ Hz, marked higher harmonic contributions, and detectable content up to 50 Hz. The relatively low frequency where the dominant peak is found reflects the characteristic frequencies of the active filters, namely $f = \{3.4, 7.2, 3.4\}$ Hz (neglecting the non-linear path), and is also influenced by the temporal scale at which the memristor non-linearity fully develops, considering that the linear loop itself would not oscillate in isolation. Qualitatively, the time-series for $v_1$, $v_2$ and $v_3$ appeared sine-like, whereas that for $v_4$ featured positive spikes having large and variable amplitude, and appearing in the form of sudden divergence from the positive half-wave (Figs. 3a and 4a). Due to the amplitude fluctuations, the current-voltage plot for the memristor consisted not of a limit-cycle loop but was "filled" and thus acquired a peculiar butterfly-like appearance, whose wings were considerably more asymmetric for the carbon-based device (Fig. 4c) than the tungsten-based device (Fig. 3c). The projections of the attractor onto several planes (Figs. 3d-h and 4d-h) illustrated its spiral, phase-coherent structure, which was reminiscent of paradigmatic cases such as the Rössler system [39]. Crucially, saturation never occurred at any node in this circuit, the measured voltages remaining well below the supply rails; the only infrequent exceptions were excessively large positive spikes at node $v_4$, found exclusively for the carbon-based memristor circuit, which were well-separate and occurred only for isolated cycles.

To confirm the chaotic behavior of the circuit, the entire spectrum of Lyapunov exponents $\lambda_1 \dots \lambda_4$ was calculated (values reported verbatim without normalization), from which the Kaplan-Yorke dimension $D_{KY}$ was obtained. Since voltages corresponding to the four state variables were directly accessible, time-lag embedding could be skipped, parsimoniously avoiding any assumptions about the lag $\delta$ and order $m$. Instead, the state vector was expressed directly as $\mathbf{x} = \{v_1, v_2, v_3, v_4\}$, and the method of Sano and Sawada [40], as implemented in the `TISEAN` package (ver. 3.0.1) [41,42], was applied. To attenuate the effects of noise and discretization, the time-series, which were initially considerably oversampled, were smoothed via a moving average of 20 points, detrended, and finally decimated by a factor of 10. The Lyapunov exponents were independently estimated over 8 segments of 30,000 points each, from which the average was taken, and the standard deviation was assumed as an estimate of random error.

For the case of the tungsten-based memristor (Fig. 3), $\lambda_1 = 0.011 \pm 0.003$, $\lambda_2 = -0.004 \pm 0.001$, $\lambda_3 = -0.032 \pm 0.005$, and $\lambda_4 = -0.10 \pm 0.02$, yielding $D_{KY} = 2.21 \pm 0.09$. Using the carbon-based memristor (Fig. 4), $\lambda_1 = 0.019 \pm 0.005$, $\lambda_2 = 0.002 \pm 0.001$, $\lambda_3 = -0.06 \pm 0.02$, and $\lambda_4 = -0.41 \pm 0.05$, yielding $D_{KY} = 2.40 \pm 0.22$. In both cases, $\lambda_1 > 0$, confirming chaoticity, furthermore $\lambda_2 \approx 0$, which, allowing for possible biases while calculating the Lyapunov exponents from experimental data, agrees with the predicted presence of one zero exponent. The attained attractor dimension, $D \approx 2$, was indicative of low-dimensional chaotic dynamics.

## 4. Mathematical model

Realistic memristor modeling is an intricate issue addressed with approaches of different complexity and accuracy. Very accurate accounts capture the physical processes occurring in the device, making it possible to simulate the behavior under a wide range of realistic scenarios. However, such models usually include many parameters that are difficult to tune, and result in a heavy computational load when instanced in an oscillating circuit [43–45]. For this reason, more compact models, suitable for use with mainstream circuit simulators and equation solvers, have been developed; they provide a stylized behavioral description in terms of the *i-v* device characteristics, and are often derived under the idealized assumption of symmetric drive [46–48]. This represents a potential obstacle because, in experimental scenarios particularly for autonomous circuits, the application of a non-zero average voltage may quickly occur due to offsets or saturation, and unavoidably cause a drift in the non-volatile device parameters.

A broad range of models suitable for differential equation- and SPICE-based simulation have been introduced and are comprehensively reviewed in Ref. [49]. Here, as the focus was not on numerical simulation but obtaining an experimentally-viable chaotic oscillator using an empirical approach, no efforts were targeted at determining the most appropriate one among the available models. We outright adopted the mean metastable switch (MMS) memristor model, a stochastic representation specifically developed to fit the self-directed channel memristor properties and advised by the manufacturer [50,51]. For brevity, here we only report numerical simulations of the equation-based model, but similar results could

be obtained with the LTSpice circuit simulator, and the corresponding netlist is available in Ref. [38].

According to this model, the conductance of the memristor is described by $G = w/R_{ON} + (1-w)/R_{OFF}$, where $R_{ON}$ and $R_{OFF}$ are the on and off resistances of the device, and $w \in [0, 1]$ is a dynamical variable accounting for its internal state. The memristor current is given by

$$i^{(M)} = (w/R_{ON} + (1-w)/R_{OFF})v^{(M)}. \tag{3}$$

The dynamics of the memristor internal variable are represented as

$$\frac{dw}{dt} = \frac{1}{\tau} f\left(v^{(M)}, w\right), \tag{4}$$

where

$$f(x,w) = \frac{1-w}{1+e^{-(x-V_{ON})/V_T}} - w\left(1 - \frac{1}{1+e^{-(x+V_{OFF})/V_T}}\right) \tag{5}$$

Here, $V_T = q/KT$ with $q$ being the elementary charge, $K$ the Boltzmann constant and $T$ the temperature, while $\tau$, $V_{ON}$, and $V_{OFF}$ are three further model parameters representing the device time constant and the hysteretic threshold voltages. In the simulations which follow, we assumed $V_T = 25.7$ mV and, to empirically represent the properties of the tungsten-based memristor in the proposed circuit, we fixed $R_{ON} = 5$ kΩ, $R_{OFF} = 100$ kΩ, $\tau = 0.1$ ms, $V_{ON} = 0.50$ V and $V_{OFF} = 0.40$ V; these settings are not critical.

The system in Eq. (1) can be rewritten as

$$\begin{cases} \frac{dv_1}{dt} = \frac{1}{RC_1}\left(-\frac{R}{R_4}v_1 - \frac{R}{R_9}v_2 - \frac{R}{R_3}v_4\right) \\ \frac{dv_2}{dt} = \frac{1}{RC_1}\left(-\frac{C_1}{C_3}\frac{R}{R_8}v_2 - \frac{C_1}{C_3}\frac{R}{R_7}v_3\right), \\ \frac{dv_3}{dt} = \frac{1}{RC_1}\left(-\frac{C_1}{C_2}\frac{R}{R_5}v_1 - \frac{C_1}{C_2}\frac{R}{R_6}v_3\right) \end{cases} \tag{6}$$

wherein $R = 1$ kΩ represents a fictitious resistor introduced for rescaling the physical variables into dimensionless quantities. In particular, we consider $y_1 = v_2/\mathrm{V}$, $y_2 = v_3/\mathrm{V}$ and $y_3 = v_1/\mathrm{V}$, alongside a rescaled time $\hat{t} = \hat{\tau}t$, with $\hat{\tau} = RC_1$.

Let us also introduce the following dimensionless parameters

$$\begin{aligned} a_{11} &= -\frac{C_1}{C_3}\frac{R}{R_8} & a_{12} &= -\frac{C_1}{C_3}\frac{R}{R_7} \\ a_{22} &= -\frac{C_1}{C_2}\frac{R}{R_6} & a_{23} &= -\frac{C_1}{C_2}\frac{R}{R_5} \\ a_{31} &= -\frac{R}{R_9} & a_{33} &= -\frac{R}{R_4}, \\ b &= \frac{R_{11}}{R_{10}} & c &= \frac{R}{R_3} \end{aligned} \tag{7}$$

from which one gets

$$\begin{aligned} \frac{dy_1}{d\hat{t}} &= a_{11}y_1 + a_{12}y_2 \\ \frac{dy_2}{d\hat{t}} &= a_{22}y_2 + a_{23}y_3, \\ \frac{dy_3}{d\hat{t}} &= a_{31}y_1 + a_{33}y_3 - cu \end{aligned} \tag{8}$$

wherein

$$u = -by_2\left(1 + w\frac{R_1}{R_{ON}} + (1-w)\frac{R_1}{R_{OFF}}\right). \tag{9}$$

where without loss of generality we have set $U = 0$.

In addition, the equation for the dynamics of the memristor becomes:

$$\frac{dw}{d\hat{t}} = \frac{\hat{\tau}}{\tau} f(-by_2, w), \tag{10}$$

Readjusting the control parameters without loss of generality, namely setting $R_1 = 15$ kΩ and $R_3 = 4.3$ kΩ, yields the following settings for the dimensionless model: $a_{11} = -0.0303$, $a_{12} = -1$, $a_{22} = -0.0971$, $a_{23} = -2.1364$, $a_{31} = -1$, $a_{33} = -1$, $b = 2.1277$, $c = 0.2326$. This re-tuning became necessary due to the approximations introduced by the memristor model, which only captures the main non-linear features, disregarding the complex phenomena exemplified in Section 2. Another relevant factor to take into account is the lack of knowledge about the initial status of the memristor, reflected into the initial conditions of the variable $w$. As shown below, this determines different behaviors in the mathematical model.

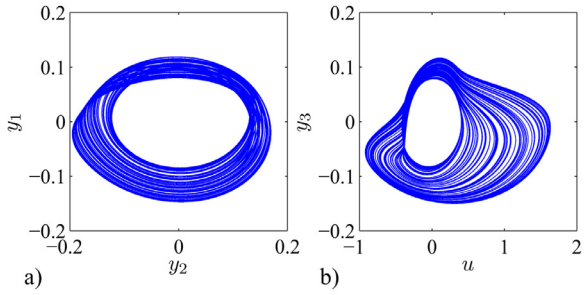


**Fig. 5.** Simulated chaotic attractor from the mathematical model of the memristor-based chaotic circuit, Eqs. (8)–(10). Projections of the attractor on the a) $y_2 - y_1$ and $u - y_3$ planes.

For these parameter settings, integrating Eqs. (8)-(10) yields the chaotic attractor shown in Fig. 5, which is qualitatively in good agreement with the experimental results presented in Section 3, albeit with slightly different geometry. To confirm chaoticity, the spectrum of Lyapunov exponents was obtained directly from the differential equations and linearization of the system, via solving the corresponding variational equation and iteratively applying the Gram-Schmidt orthonormalization [52]. The system was integrated with the explicit Runge-Kutta (4,5) pair [53], setting relative and absolute precision to $10^{-8}$ and $10^{-10}$ respectively, up to $t_{max} = 100/(RC_1)$. The initial conditions were set to $y_1 = 0.2$ and $y_2 = y_3 = w = 0$. Chaoticity was confirmed via obtaining $\lambda_1 = 0.086 \pm 0.001$, $\lambda_2 = -0.0004 \pm 0.0004$, $\lambda_3 = -0.787 \pm 0.002$, and $\lambda_4 = -4.036 \pm 0.056$. The corresponding Kaplan-Yorke dimension was $D_{KY} = 2.11 \pm 0.01$, which is remarkably close to the values observed experimentally.

Notably, removing the resistors $R_6$ and $R_8$ from the circuits yields $a_{11} = a_{22} = 0$, such that the governing equations can be rewritten in a jerk-like form [54]

$$\dddot{y} - a_{33}\ddot{y} - a_{12}a_{23}y + a_{12}a_{23}cu = 0, \tag{11}$$

with $y = y_1$ and wherein chaos could be readily recovered by adjusting the setting of a single parameter, namely, $R_{10} = 37$ kΩ, or $b = 2.703$.

A systematic analysis of the model behavior was carried out by numerically calculating the bifurcation diagrams for the parameters $b$ and $c$. The results are shown in Fig. 6a and b for the full model and in Fig. 6d and e for the jerk-like version. These diagrams reveal an evident period-doubling route to chaos, with intertwined narrow windows of periodicity. The chaotic attractor disappears through a crisis due to the stabilization of a fixed point. Quite interestingly, the system behavior strongly depends on the initial condition of the memristor internal variable, such that, for instance, the crisis bifurcation point changes with $w(0)$. This feature appears in other chaotic systems based on memristors and now confirmed in a real experiment model, leading to two significant characteristics, i.e., multistability and bifurcation without parameters [55]. The latter is highlighted in Fig. 6c and f, wherein the system behavior is studied varying $w(0)$ while maintaining fixed parameter settings. At distinct values of $w(0)$, the system may display totally different behaviors: for example, it may bifurcate from stable equilibrium to chaos and viceversa (Fig. 6c), or generate

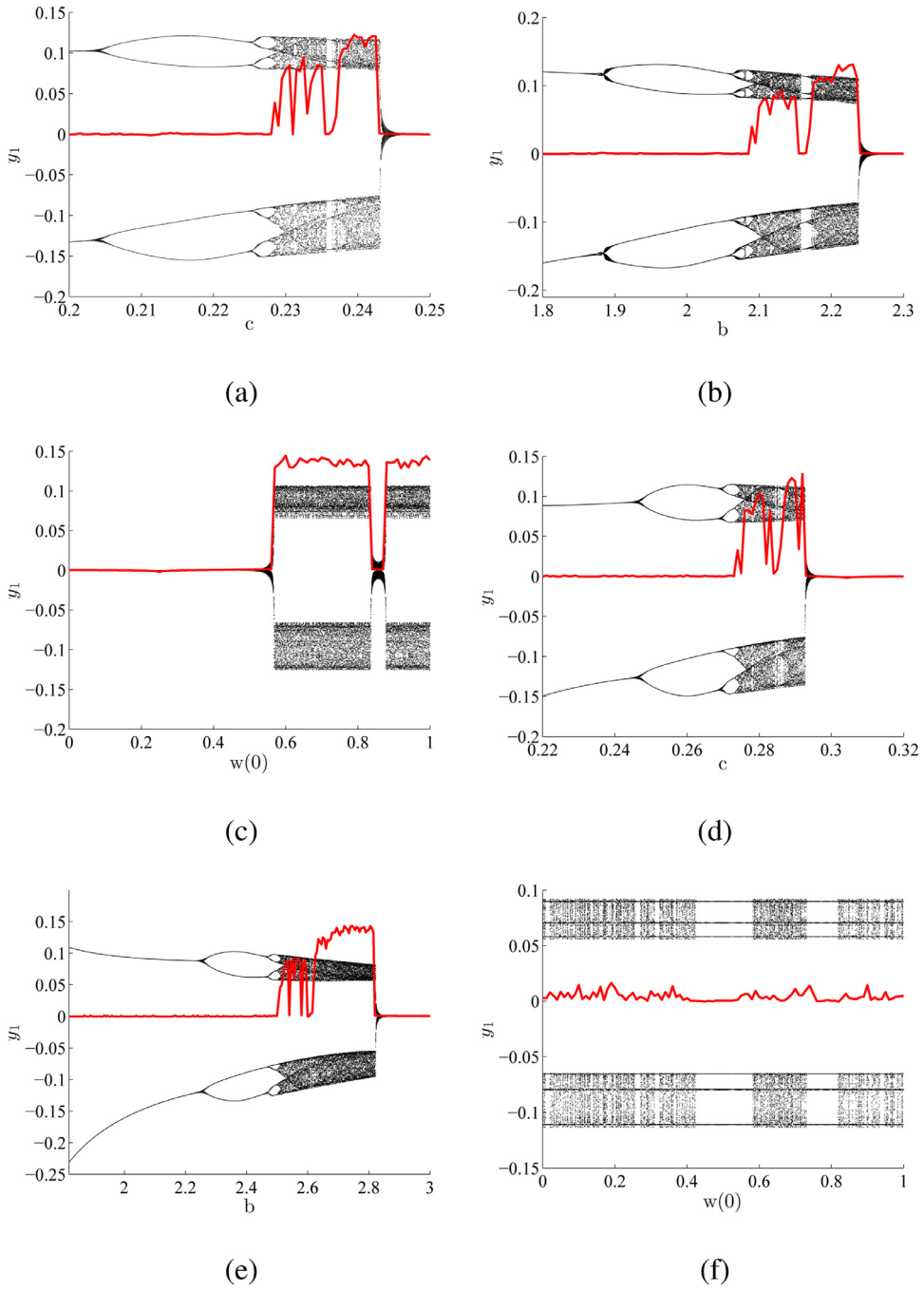


**Fig. 6.** Bifurcation diagrams (in black) and maximum Lyapunov exponent (in red) from the models of the memristor-based chaotic circuit. a) and d) Bifurcation with respect to parameter $c$, keeping $b = 2.1277$. b) and e) Bifurcation with respect to parameter $b$, keeping $c = 0.2326$. c) and f) Bifurcation without parameters: all model parameters fixed ($b = 2.3$ and $c = 0.2326$ in c, $b = 2.614$ and $c = 0.2326$ in f), while the initial condition of the memristor internal variable $w(0)$ is varied. For panels a-c), which stem from the full model, $a_{11} = -0.0303$ and $a_{22} = -0.0971$; for panels d-(f), which refer to the jerk-like mode, $a_{11} = a_{22} = 0$. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

windows of periodicity intercalated with weakly chaotic behavior (Fig. 6f).

Another remarkable consideration that emerges from the analysis of the bifurcation diagrams in Fig. 6 is the extent of the region wherein chaotic behavior appears. Referring, for instance, to the bifurcation diagram with respect to parameter $c$ (Fig. 6a), we notice that chaos appears for $c \in [0.23, 0.24]$, which corresponds to quite a narrow interval of the corresponding physical parameter, namely, $R_3 \in [4170, 4350]$. This contrasts with the results from Ref. [37], wherein a robust chaotic circuit was obtained from a circuit architecture involving two feedback loops and a single non-linear component realized by a diode, and suggests that the non-linearity plays a prominent role in determining the circuit robustness. The physical memristors under consideration appear able to generate chaos, however, future devices with improved non-linear characteristics could lead to a more robust chaotic circuit.

## 5. Conclusions

The interest in memristors as foundational elements for chaotic oscillators flows from multiple directions. On the one hand, as elaborated in Sec. I, they are the only fundamental two-terminal

electronic component that is non-linear. On the other hand, they also have an inherent appeal as building blocks of complex systems and networks from a multidisciplinary perspective. In natural systems, from the scale of a cell receptor through that of a brain and eventually an entire ecosystem, non-linearity and memory are both fundamental and pervasive features. The relationships between physical, such as physiological, variables are almost invariably non-linear, and adaptability is eventually always subserved by means through which dynamics can impart a lasting impact on the structural properties of a system such as its parameters, as observed, for example, from synaptic plasticity all way up to the diversified evolution of species [56–58]. Because resistors, inductors and capacitors are all linear and static in their physical properties, memristors acquire, at least in principle, a unique relevance in bridging electronic engineering towards paradigms closer to true biological inspiration. Of note, semiconductors such as diodes, alongside countless other devices such as gas-discharge tubes, readily offer a vast catalog of non-linear relationships, but the intrinsic memory aspect remains lacking [59].

The simple memristor-based chaotic circuit discussed in this paper was designed following a bottom-up approach, which was predicated upon an experimental investigation of the realistic device features. Many of these can be elusive to model but are nevertheless crucial for obtaining a viable oscillator. The inability to observe the internal variable, and the manufacturing variability alongside non-volatile, even partially irreversible, changes further reduce the practical usefulness of memristor behavioral models in illuminating the way towards the design of a circuit that functions when experimentally realized. Physics-based models do not alleviate this problem substantially, because their greater realism requires assumptions regarding a large number of parameters, which are in themselves highly variable and not straightforward to measure. In the case of the present study, pursuing a search-based approach such as the one which was successfully applied to the design of transistor-based chaotic circuits in Ref. [60], produced configurations most of which, in the laboratory, even failed to sustain oscillation (not reported herein for brevity). This situation motivated the choice of a bottom-up strategy. The search for a suitable architecture was not trivial, as many attempts generated circuits wherein there was no chaotic behavior, or the memristor underwent irreversible changes or played no discernible role, for example because of the onset of saturation. Although only anecdotal, our experience suggests that the use of physical memristors even in well-behaved chaotic architectures such as Saito's circuit [61], is far from straightforward. The architecture based on two feedback loops, introduced in Ref. [37], appeared to combine some desirable features for realizing a memristor-based chaotic circuit. In this respect, it should be clear that the purpose of this study was neither attempting to improve it, nor reaching any general conclusion regarding methods for designing a memristor-based chaotic circuit, nor conducting a systematic investigation across multiple topologies. More modestly, we aimed to identify one self-contained autonomous circuit suitable for generating chaos using as the sole source of non-linearity a physical memristor.

It appears noteworthy that the architecture introduced in Ref. [37] could be used to design a memristor-based chaotic oscillator simply by replacing the diode in the original configuration with a first-order memristive diode bridge as shown in Ref. [23]. However, while such a diode bridge is a memristive system [62], the converse is not true since real memristors, in general, are not diode bridges. Hence, while a diode bridge-based memristive system can be straightforwardly used in the original configuration of Ref. [37] in place of the single diode to obtain a chaotic circuit, the same is not true for the self-directed channel physical memristor, which instead required significant changes in the configuration. This juxtaposition confirms that using a real memristor is a conceptually different task compared to instancing idealized models or electronic analogues of the same.

Although the proposed circuit contains multiple operational amplifiers, chaos has to be uniquely attributed to the non-linearity of the memristor. When working outside of their linear operating region, operational amplifiers might elicit a non-linearity strong enough to generate chaos, as, for instance, occurs in the cellular non-linear network implementation of the Chua's circuit [63]. Here, this possibility was excluded through comprehensive recording and monitoring of all circuit nodes. Further confirmation of the central role of the memristor non-linearity comes from the mathematical model of the circuit, which assumes that all amplifiers operate linearly and yielded chaotic behavior qualitatively similar to the experimental observations. Another degenerate possibility that should be mentioned is that the memristor could be operating as a static non-linearity, similarly, for example, to a diode. A concern arises because the circuit contains three capacitors and, therefore, in itself possesses sufficient dimensionality for chaos generation even without the internal state variable of the memristor. It is, however, readily dissipated by observing the characteristic pinched hysteresis loops, additionally enriched by the chaotic dynamics, which evidently do not delineate a relationship between the memristor voltage and current that could be ascribed to a function, even a non-linear one: as expected, a time-dependency of the non-linearity is present, indicating that the device behaviour cannot be trivially accounted for by a function, but requires a functional.

In summary, our results provide experimental evidence of the suitability of currently commercially-available memristors for building an autonomous chaotic circuit. This motivates their consideration for use in other chaotic architectures, including those based on more than one memristor [29], and, more importantly, in the broader context of non-linear dynamics. For instance, recent theoretical results indicate that adaptive consensus and synchronization could be reached in networks of dynamical systems coupled via memristors [64,65]. On the other hand, it should be acknowledged that the low-dimensional dynamics observed here are characterized by features largely overlapping with the phase-coherent attractors readily generated by some previously well-known circuits, such as single-transistor oscillators, which are also structurally considerably simpler [60,66]. Nevertheless, our results pave the way for convenient small-scale laboratory experimentation of memristor-based circuits with adaptive parameters, and additionally have notable educational value in finally providing a platform for demonstrating the possible practical use of memristors in chaos generation.

## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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