A New Electronic Timer

by

P.L. Nonn and J.C. Sprott

February 1968

PLP 179

Plasma Studies
University of Wisconsin

In pulsed plasma experiments, it is often necessary to have trigger pulses at various adjustable times. In the course of developing a self-contained magnetron control unit for use on the octupole, the timer circuit described herein was designed and constructed.

Fig. 1 shows a schematic diagram of the timer. The input trigger signal (either external or internal) closes SCR 1 causing capacitor C_1 to discharge through the zener diodes Z_1 and Z_2 producing a 30 volt square pulse which is used to charge capacitor C_2 through the variable resistor R_1. R_2 is adjusted so that after a time $\tau = R_1C_2$, the voltage across C_2 becomes sufficient to fire the unijunction transistor which discharges C_2 into R_3 and fires SCR 2 which discharges C_1 and C_3 into the output resistor R_4.

The part of the circuit enclosed by dotted lines in Fig. 1 is constructed on a printed circuit board and can be reproduced from a photographic negative. Fig. 2 shows the layout of the PC board.

Because of the large variation in holding current for SCR's of the same type, it is necessary to choose suitable SCR's from a large batch. If the holding current is too low, the timer will not reset. For proper temperature compensation, a mylar capacitor should be used for C_2. The timer covers a range of 2 orders of magnitude. For greater range, additional choices of C_1 are needed, but the minimum delay, due to stage delay in the two SCR's is $\sim 4\ \mu$ sec. The ranges can be made integral multiples of one another by hand-choosing capacitors or by inserting a trimmer capacitor in each range except in the range with the longest delay.

The biggest advantage of this timer circuit over other circuits currently in use is that over a considerable range (down to ~ 2% of the full scale), the delay time can be read directly off the ten turn vernier dial.

A four-channel version of the timer has been constructed and is shown pictorially in Fig. 3. This unit covers the interval 10 μsec - 10 msec in two ranges. The total cost of parts if bought singly from Allied is ~ $40/channel.

Tests made on a representative channel of this timer revealed the specifications listed below:

Input	
Impedance	35 K
Minimum level	+100 V
Minimum pulse width	2 μsec
Output	
Impedance	4 Ω
Voltage	+300 V
Rise time	$<$ 0.1 μsec
Decay time (unterminated)	10 μsec
Power	
Voltages	+300, +150
Idling current	$<$ 0.1 ma
Charging current	13 ma
Recycle time	.25 sec
Jitter (Half width of gaussian)	.004 %
Linearity	$<$ 0.5 %

The timer is remarkably insensitive to temperature and line voltage changes. Using a simple zener regulated supply, the time interval changed by only .04% when the line voltage changed from 90 to 120 volts. A 1% change resulted when the timer module was cooled to liquid freon temperatures.

As an added feature, an interchangable PC board can be constructed which provides a repetitive output pulse with continuously variable rep rate. The circuit for the repetitive pulser is shown in Fig. 4, and is similar to the timer circuit except that the input SCR circuitry is omitted. C_3 was reduced to .01 μf in order to reduce the reset time to ~25 msec. If shorter time intervals are desired, C_3 can be reduced further (at the expense of output pulse width) or R_5 can be made smaller. The time interval is given by the time constant of R_1 and C_2 and has all the desirable features of direct readout, stability, and linearity.

Acknowledgment

We express appreciation to Tom Lovell for assistance in constructing the timer, particularly for laying-out the PC board and for preparing the drawings and photographs for this paper.

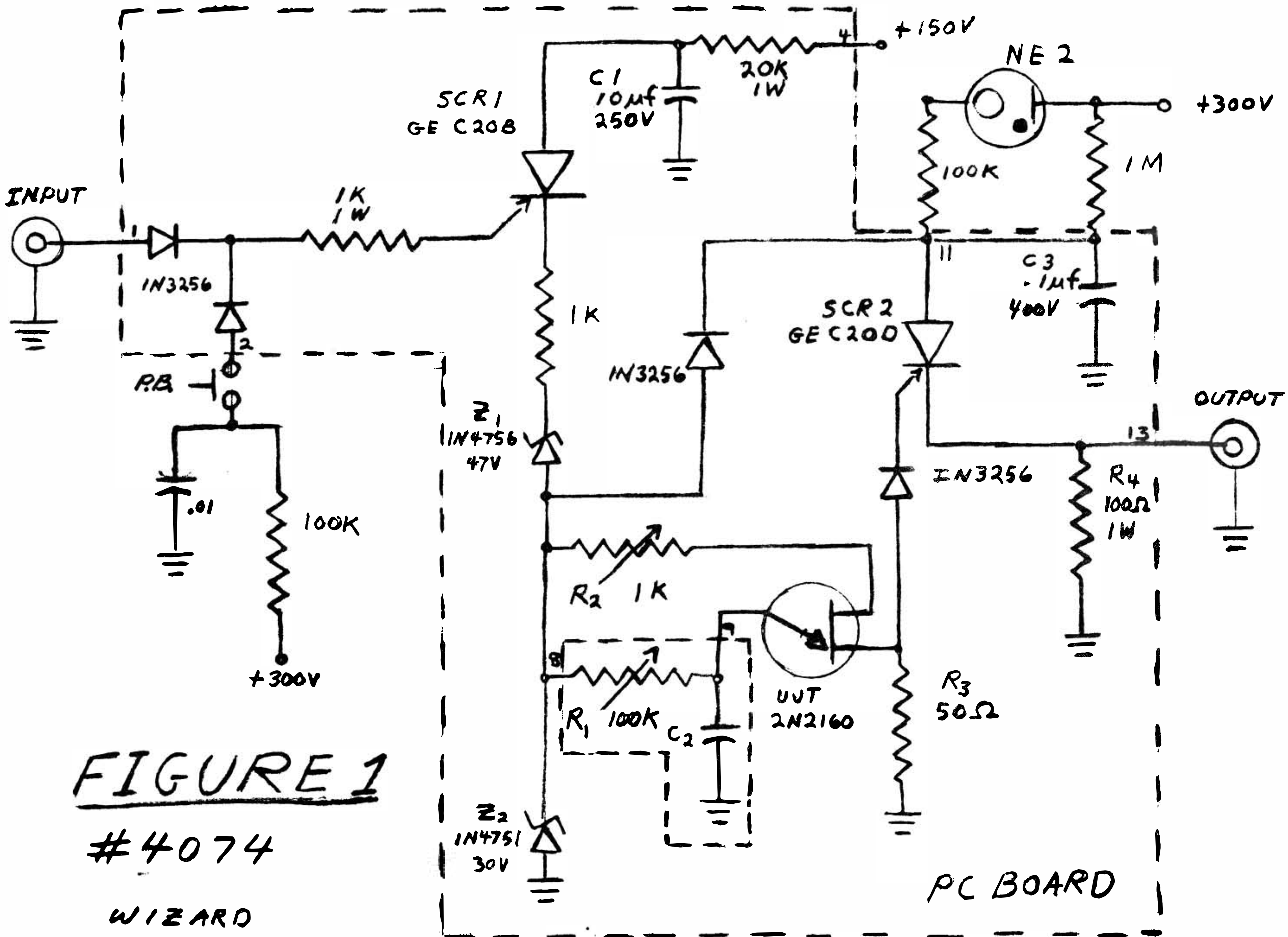

FIGURE 1

#4074

WIZARD TIMER

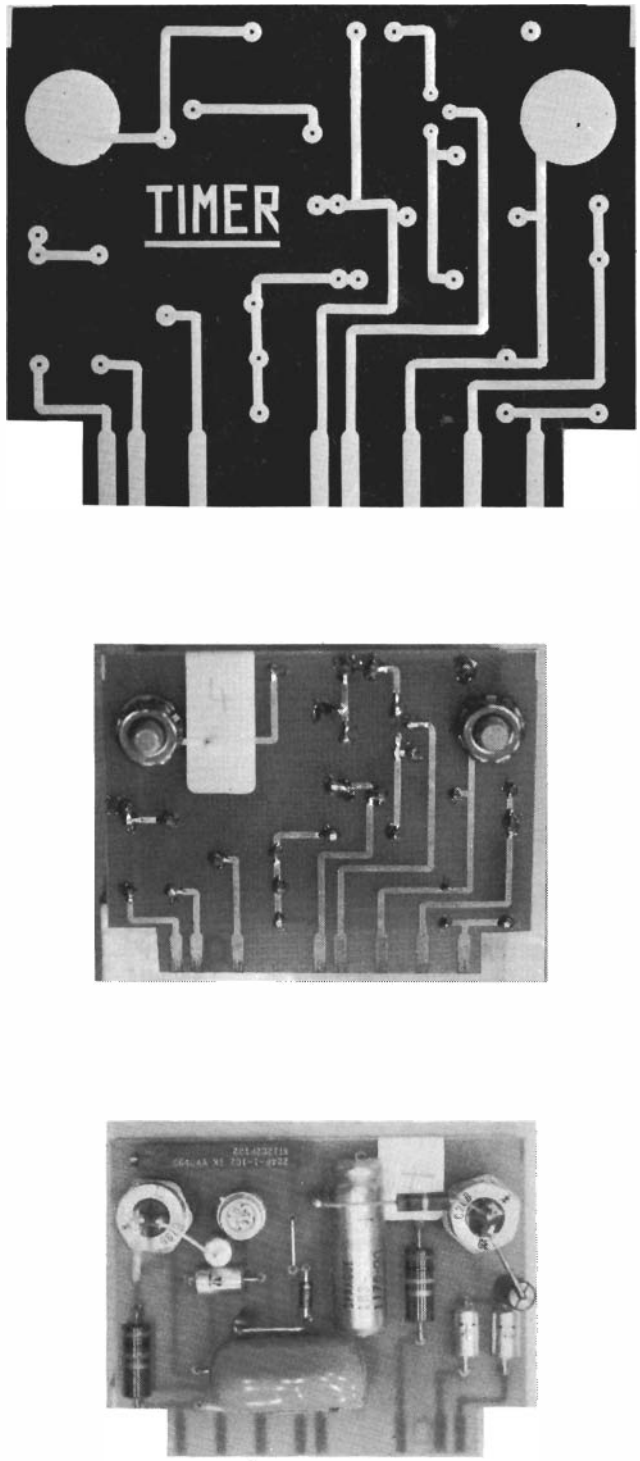

Figure 2

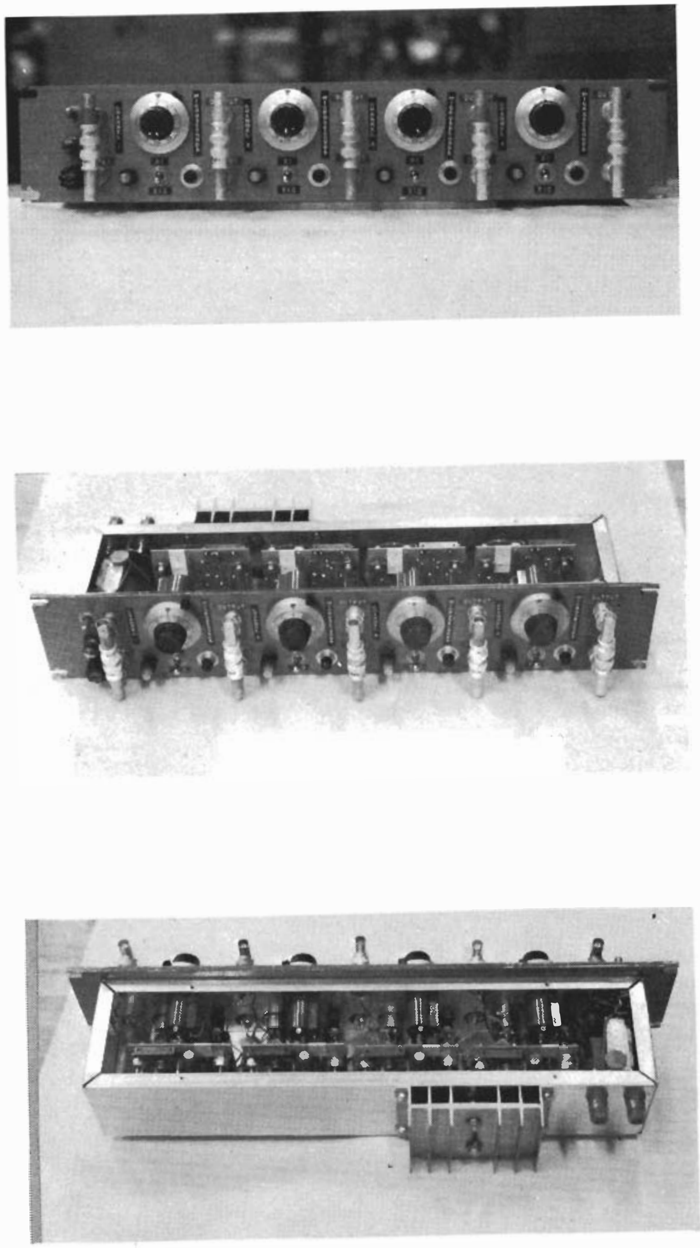

Figure 3

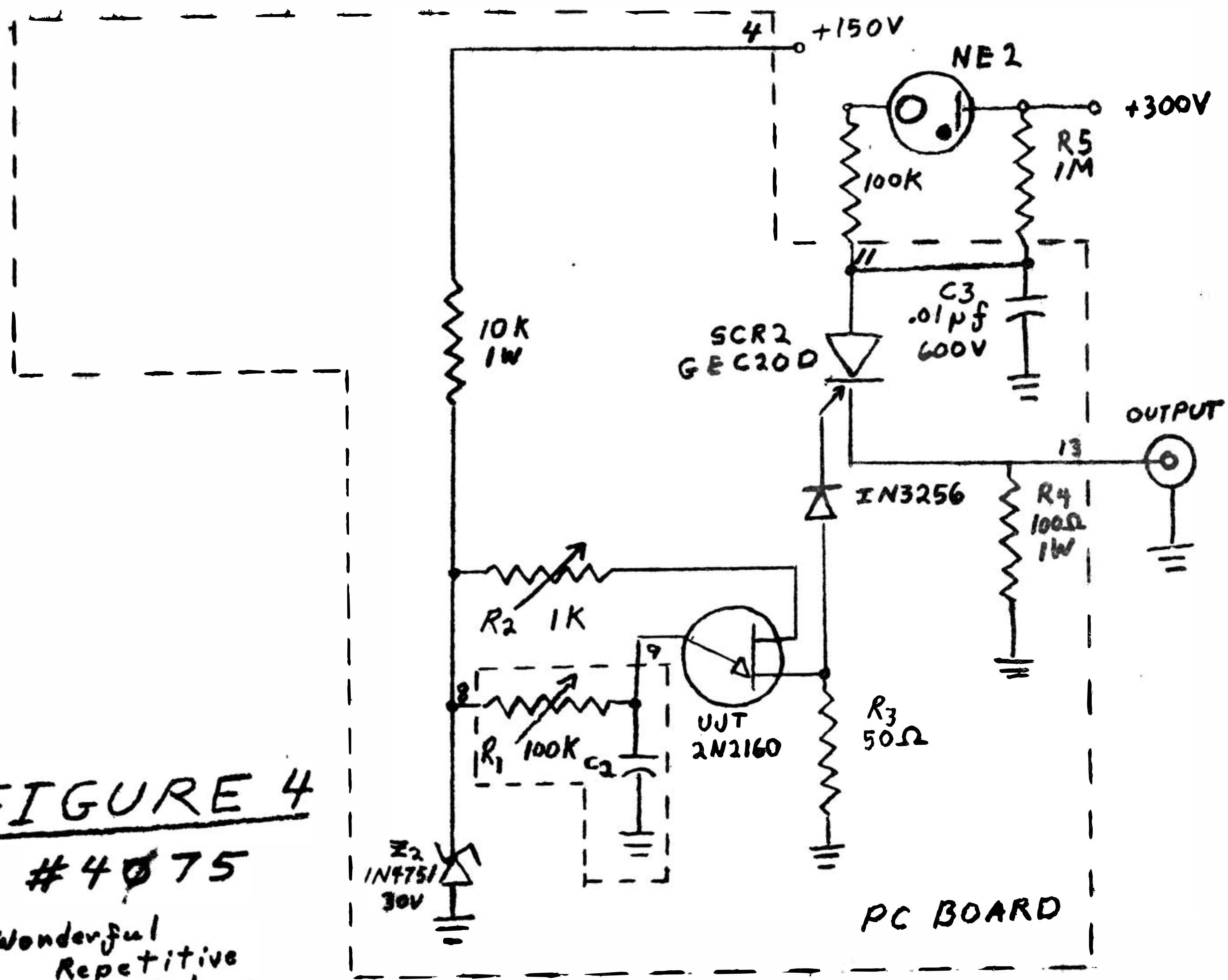

FIGURE 4

#4Ø75

Wonderful Repetitive pulser